REMARKS

Claims 1-18 are currently pending. Claims 1-10, 13, and 16-18 have been amended. No new matter is presented in this Amendment.

REJECTIONS UNDER 35 U.S.C. §103(a):

Claims 1-2, 5-6, 8-10 and 11-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Inoue (U.S. Patent 5,696,774) in view of Arai (U.S. Patent 5,757,824) and further in view of Applicant admitted Prior Art (APA).

Claims 1 and 2

It is respectfully submitted that the prior art references do not teach or suggest, individually or in combination, all of the recited limitations of claim 1. Neither Inoue nor Arai teach or suggest, individually or in combination, "an apparatus generating error flags for a data frame including a plurality of ECC (Error-Correction Coding) data blocks, wherein each ECC data block is located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error," as recited by claim 1. Thus, the rejection of claim 1 should be withdrawn for at least this reason.

Furthermore, one skilled in the art would not have been motivated to combine the error flag generator disclosed by Arai with the digital signal playback device of Inoue because the error flag generator taught by Arai is used to achieve a low-memory configuration (Arai, col. 2, lines 21-26), whereas the digital signal playback device taught by Inoue is directed at achieving a playback device which uses a large number of memories to store an increased amount of playback data (Inoue, col. 13, lines 27-31). In order to establish a *prima facie* case for obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143. A person skilled in the art trying to design an error correction apparatus which uses a single memory (Arai, col. 2, lines 21-26) would not have looked to an invention which teaches using at least nine separate memories in each structural embodiment (Inoue, col. 37, lines 11-19; Col. 42, lines 14-21; col. 44, lines 39-40). Thus, the rejection of claim 1 should be withdrawn for at least this reason as well.

Additionally, since claim 2 depends on claim 1, it is respectfully submitted that the

rejection of claim 2 should be withdrawn for at least the same reasons that the rejection of claim 1 should be withdrawn.

Claims 5 and 6

It is respectfully submitted that the prior art references do not teach or suggest, individually or in combination, all of the recited limitations of claim 5. Neither Inoue nor Arai teach or suggest, individually or in combination, the operation of "generating frame-sync error information for at least one Error Correction Coding (ECC) data block located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error, using the reproduced digital signal," as recited by claim 5. Thus, the rejection of claim 5 should be withdrawn for at least this reason.

Furthermore, one skilled in the art would not have been motivated to combine the error flag generator disclosed by Arai with the digital signal playback device of Inoue because the error flag generator taught by Arai is used to achieve a low-memory configuration (Arai, col. 2, lines 21-26), whereas the digital signal playback device taught by Inoue is directed at achieving a playback device which uses a large number of memories to store an increased amount of playback data (Inoue, col. 13, lines 27-31). In order to establish a *prima facie* case for obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143. A person skilled in the art trying to design an error correction apparatus which uses a single memory (Arai, col. 2, lines 21-26) would not have looked to an invention which teaches using at least nine separate memories in each structural embodiment (Inoue, col. 37, lines 11-19; Col. 42, lines 14-21; col. 44, lines 39-40). Thus, the rejection of claim 5 should be withdrawn for at least this reason as well.

Additionally, since claim 6 depends on claim 5, it is respectfully submitted that the rejection of claim 6 should be withdrawn for at least the same reasons that the rejection of claim 5 should be withdrawn.

Claims 8-10 and 11-17

It is respectfully submitted that the prior art references do not teach or suggest, individually or in combination, all of the recited limitations of claim 8. Neither Inoue nor Arai teach or suggest, individually or in combination, "an apparatus for generating error flags for a

data frame including a plurality of ECC (Error Correction Coding) data blocks, wherein each ECC data block is located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error," as recited by claim 8. Thus, the rejection of claim 8 should be withdrawn for at least this reason.

Furthermore, one skilled in the art would not have been motivated to combine the error flag generator disclosed by Arai with the digital signal playback device of Inoue because the error flag generator taught by Arai is used to achieve a low-memory configuration (Arai, col. 2, lines 21-26), whereas the digital signal playback device taught by Inoue is directed at achieving a playback device which uses a large number of memories to store an increased amount of playback data (Inoue, col. 13, lines 27-31). In order to establish a *prima facie* case for obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143. A person skilled in the art trying to design an error correction apparatus which uses a single memory (Arai, col. 2, lines 21-26) would not have looked to an invention which teaches using at least nine separate memories in each structural embodiment (Inoue, col. 37, lines 11-19; Col. 42, lines 14-21; col. 44, lines 39-40; FIGs. 17 and 24). Thus, the rejection of claim 8 should be withdrawn for at least this reason as well.

Additionally, since claims 9, 10, and 11-17 each depend on claim 8, it is respectfully submitted that the rejections of claims 9, 10 and 11-17 should be withdrawn for at least the same reasons that the rejection of claim 8 should be withdrawn.

Based on the foregoing, this rejection is respectfully requested to be withdrawn.

ALLOWABLE SUBJECT MATTER:

Claims 3-4, 7 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: 5/14/07

By: _____
Michael D. Stein
Registration No. 37,240

1400 Eye St., NW
Suite 300
Washington, D.C. 20005
Telephone: (202) 216-9505
Facsimile: (202) 216-951